Advanced Depleted-Substrate Transistors: Single-Gate, Double-Gate and Tri-Gate

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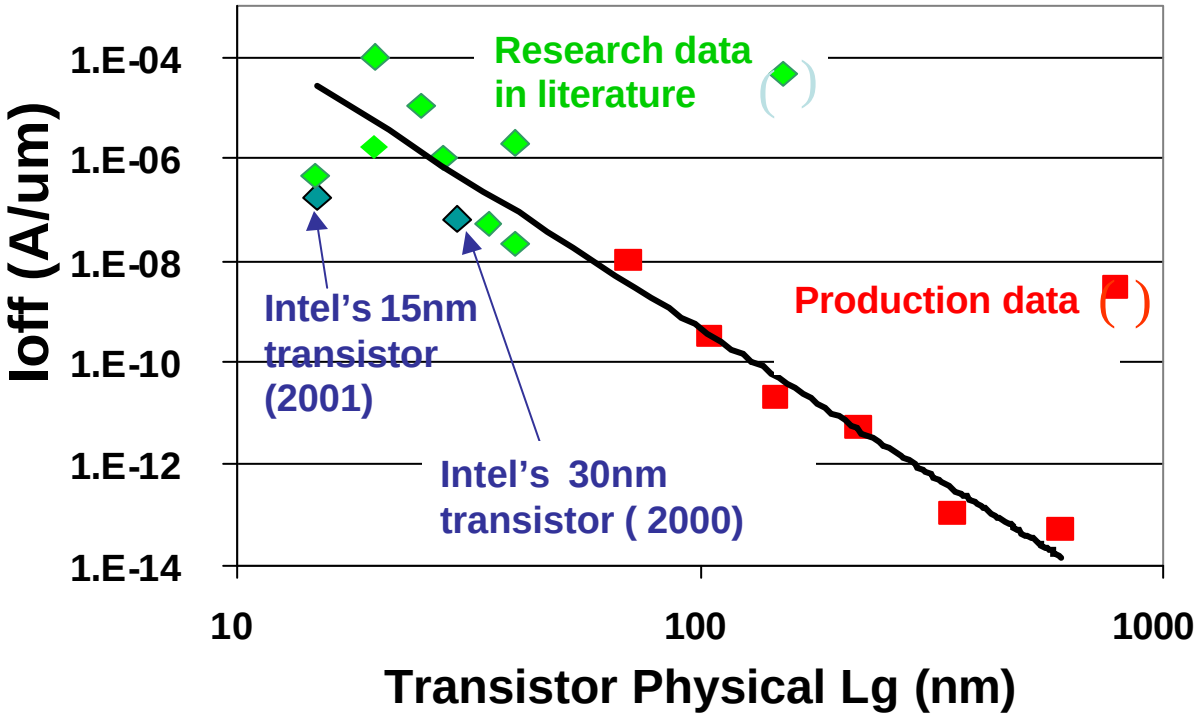
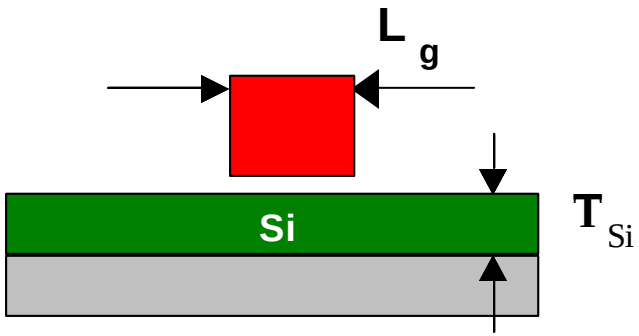
Transistor Scaling Problem: Ioff Increases with Decreasing Lg



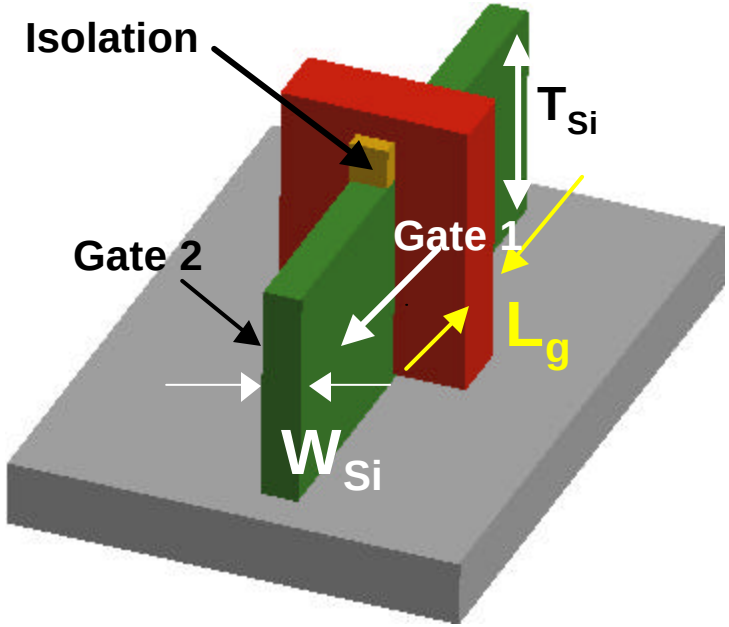
Potential Solutions:

- **Low temperature operation**
- **Improve short-channel performance (DS & DIBL) using novel device structures**
  - **Fully-Depleted Substrate Transistors (DST)**

Common Fully-Depleted Transistors

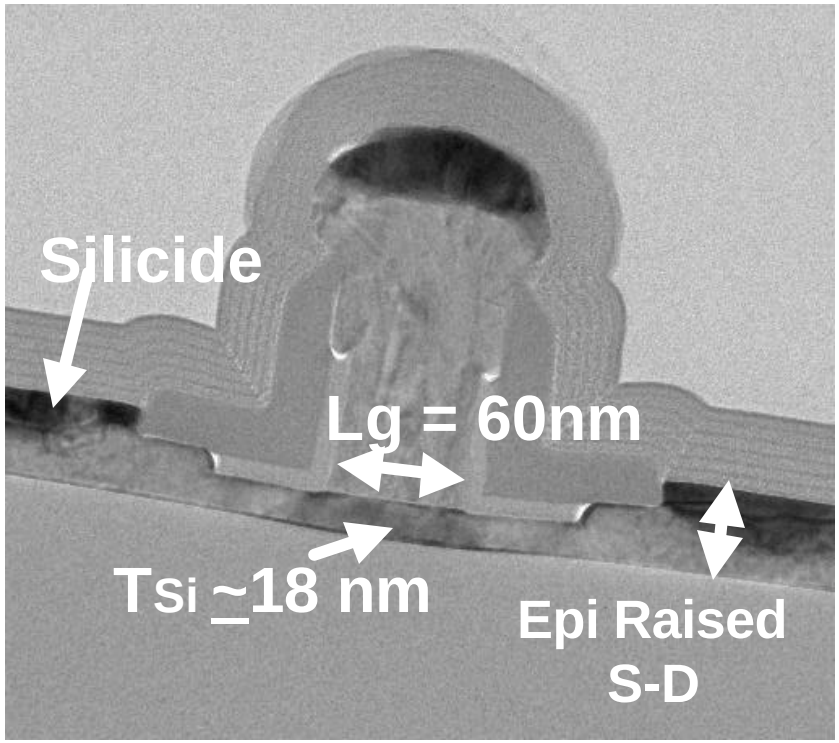


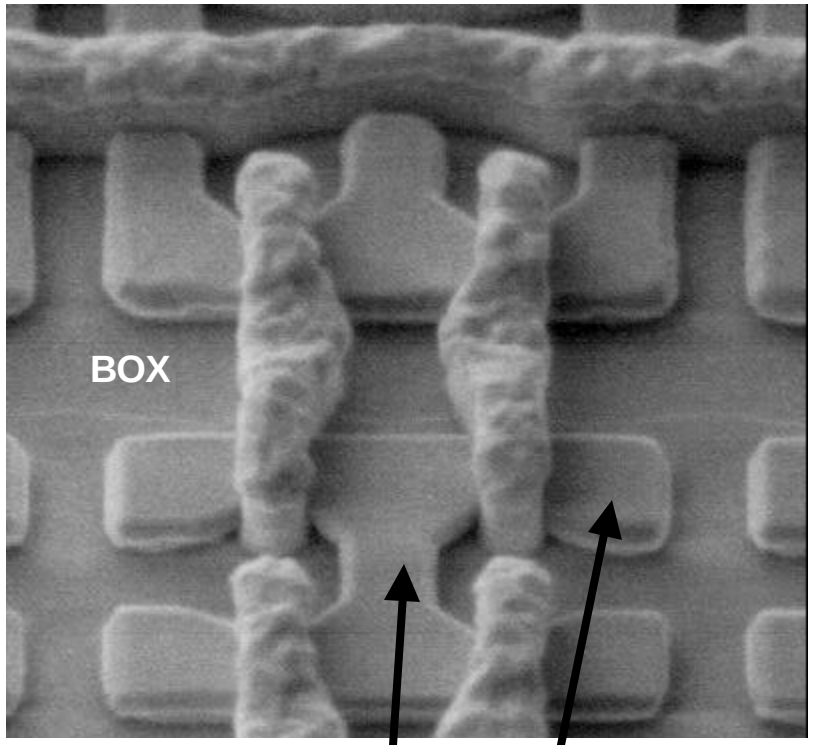
Single-gate DST = standard Fully-depleted SOI (Planar)



Double-gate (e.g. FINFET) (Non-Planar)

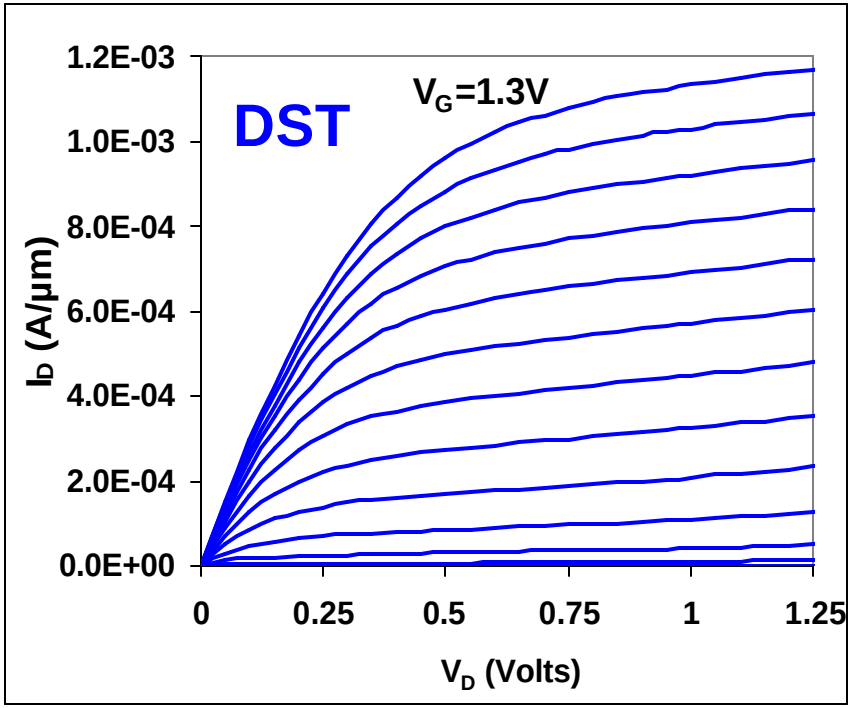
60nm Single-Gate DST Demonstrated

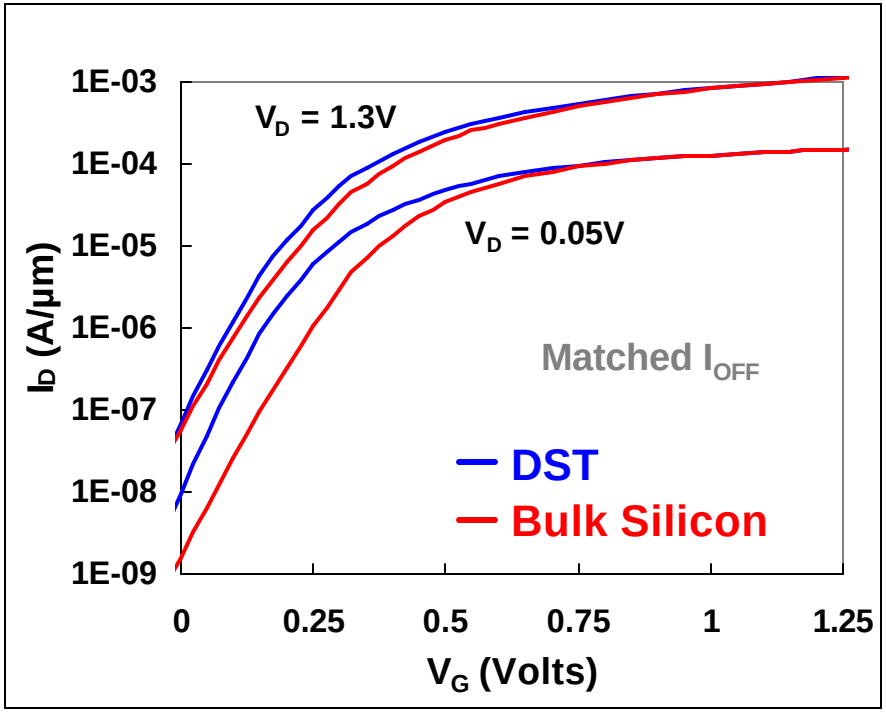




Raised S-D using Selective Epi-Si Deposition

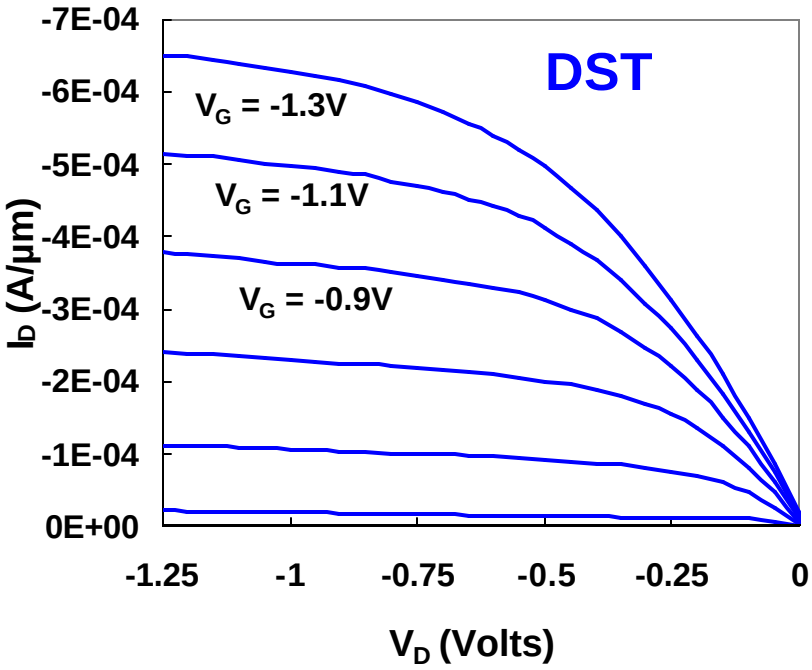
Single-Gate Fully-Depleted CMOS: NMOS

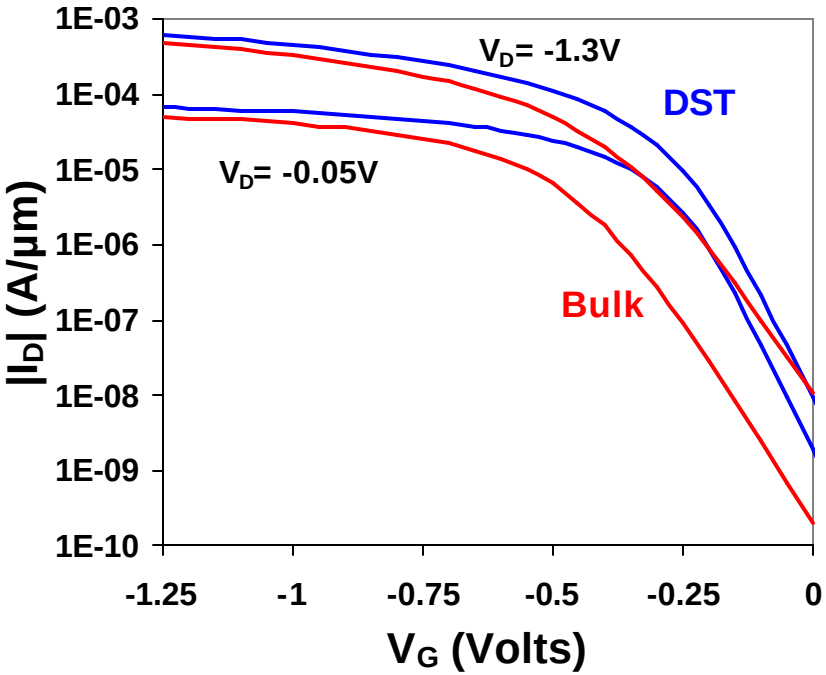




- **Excellent SCE: S.S. = 75mV/decade, DIBL = 45mV/V**
  - **for bulk Si, S.S. = 95mV/decade, DIBL = 100mV/V**
- **Excellent drive current**
  - **I_{ON} = 1.18mA/um, I_{OFF} = 60nA/um @ V_{CC} = 1.3V**

Single-Gate Fully-Depleted CMOS: PMOS

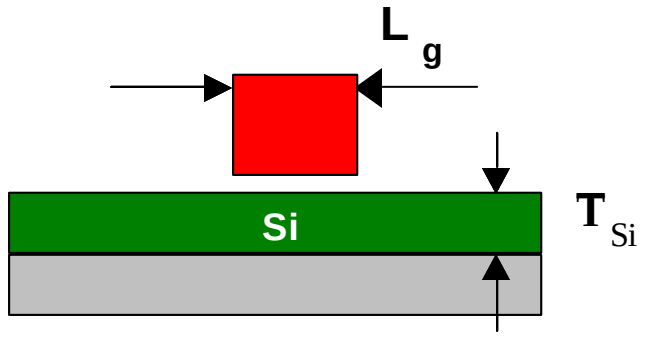




- **Excellent SCE: S.S. = 70mV/decade, DIBL = 40mV/V**
  - **for bulk Si, S.S. = 95mV/decade, DIBL = 100mV/V**
- **Excellent drive current**
  - **I_{ON} = -0.65mA/um, I_{OFF} = -9nA/um @ V_{CC} = -1.3V**

Potential Issues with Single-Gate DST

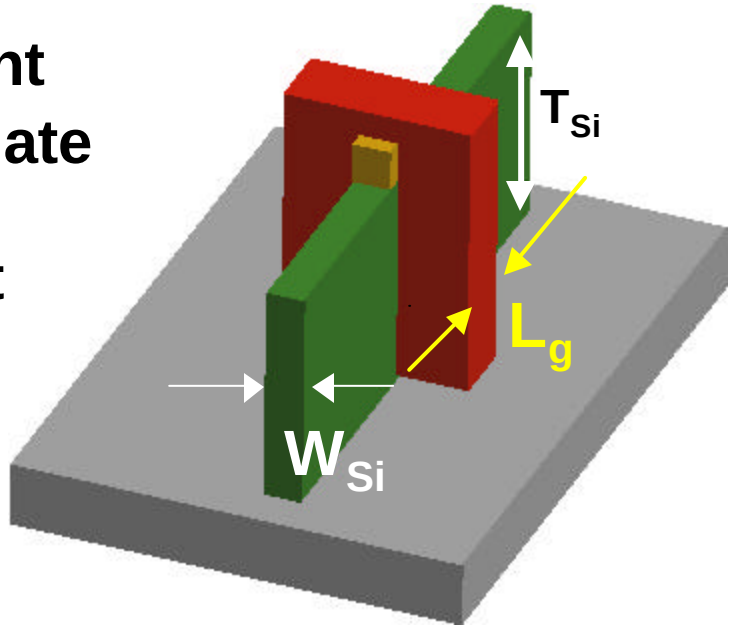
- **T_{Si} ~ Lg/3**
- **T_{Si} scales with Lg; ultra-thin Si body is required**
- **Thickness uniformity hard to control for ultra-thin Si body**



Single-gate DST = standard Fully-depleted SOI (Planar)

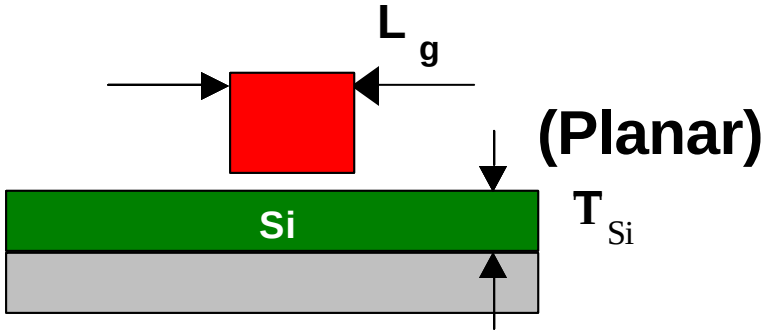
Double-Gate Fully-Depleted CMOS and its Potential Issues

- Double-gate can achieve excellent device performance like single-gate
- Difficult to fabricate; high aspect ratio
- W_{Si} ~ (2/3)*Lg; requires printing features smaller than Lg

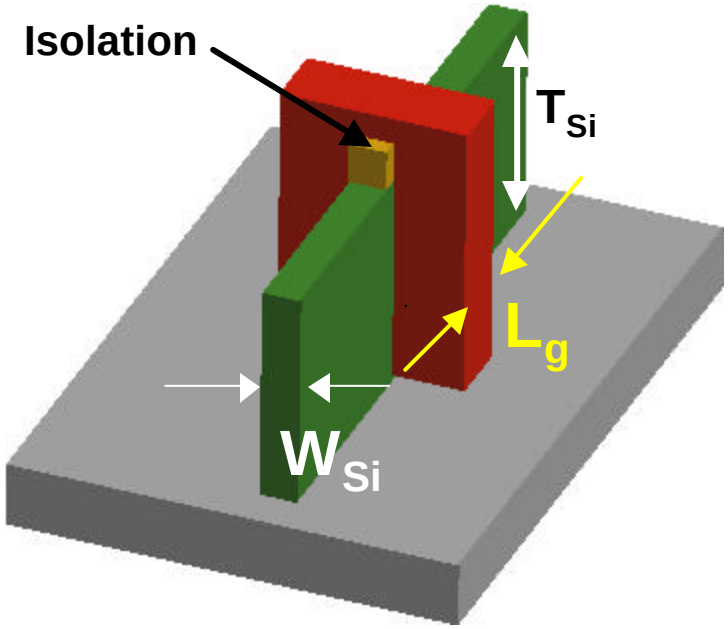


Double-gate (e.g. FINFET)

Novel Tri-Gate DST

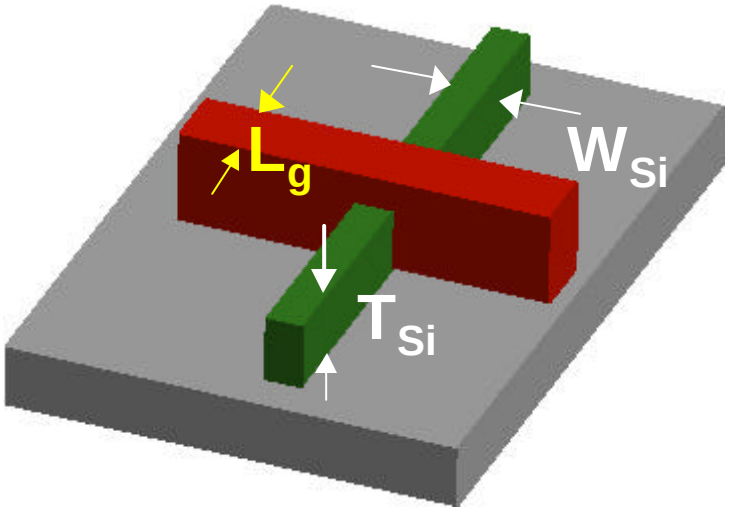


Single-gate DST = standard Fully-depleted SOI



Double-gate (e.g. FINFET)

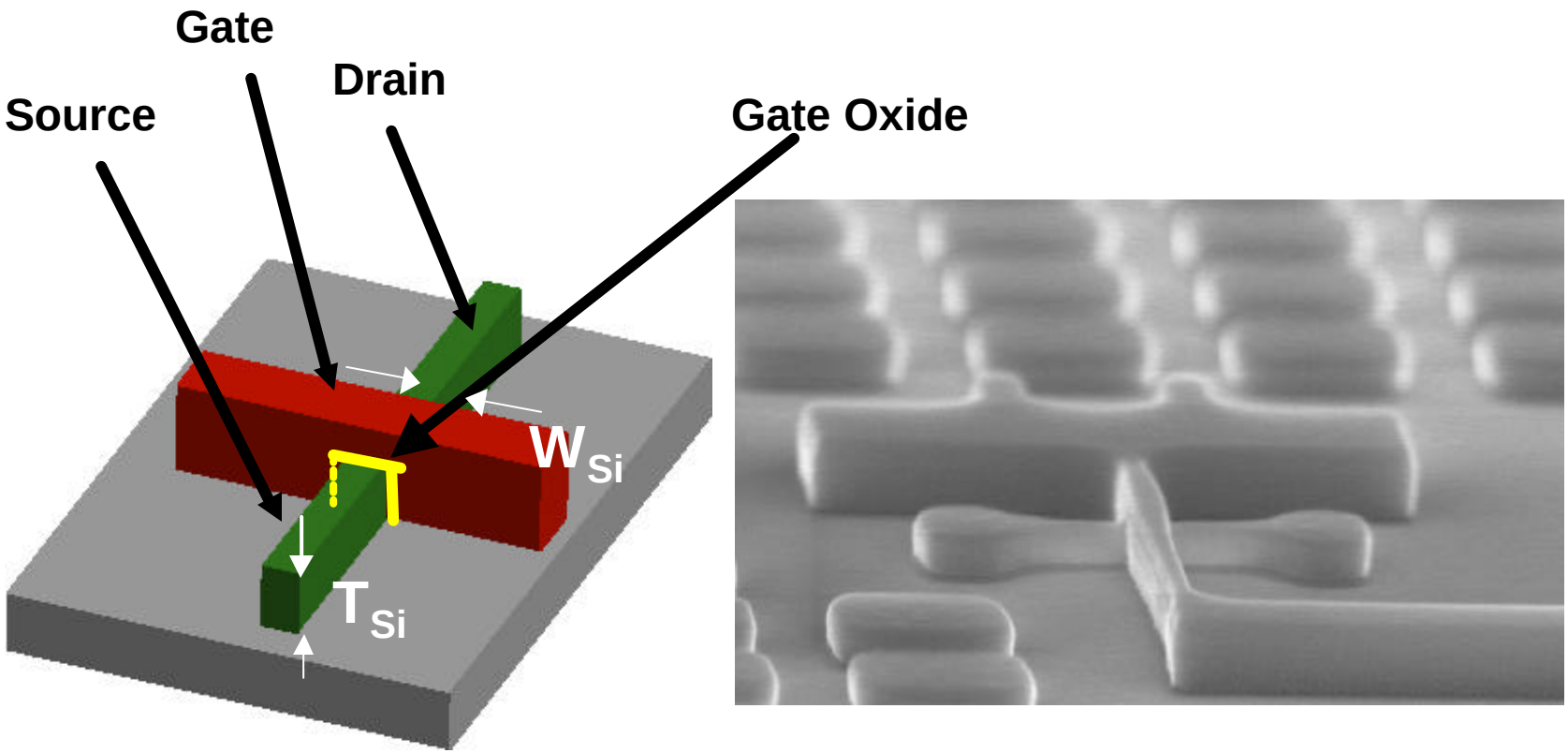
(Non-Planar)



Tri-gate DST

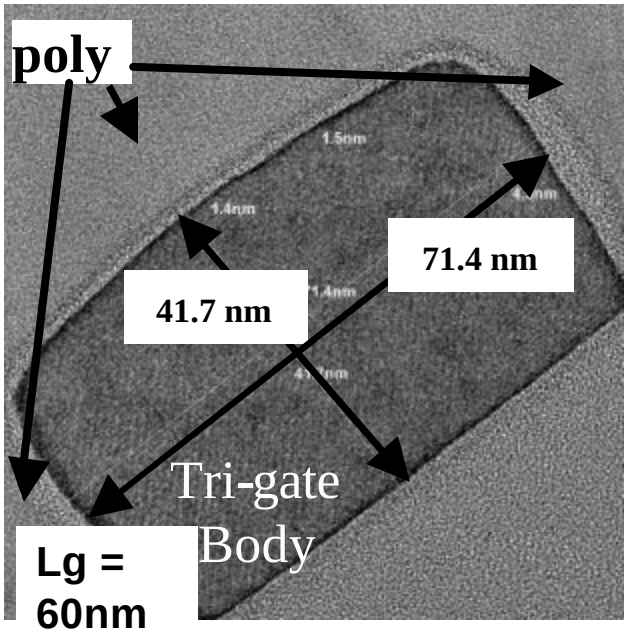
(Non-Planar)

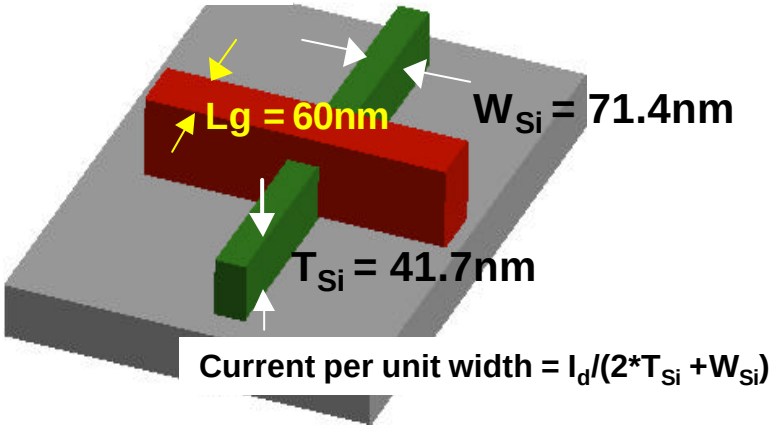
Tri-Gate DST

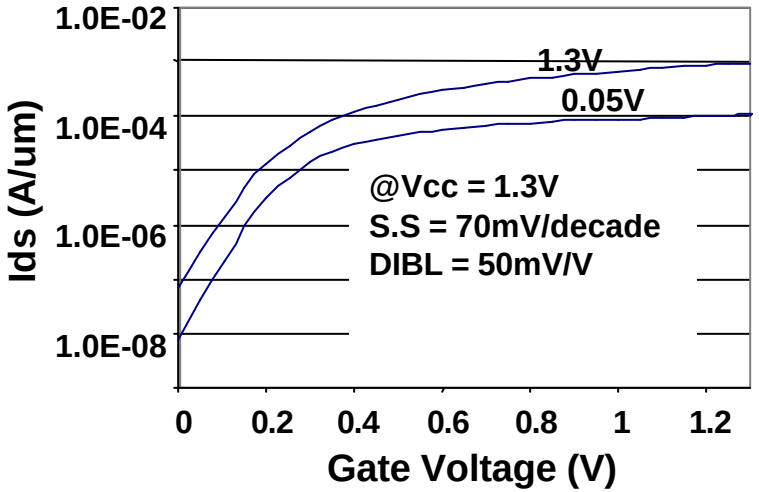


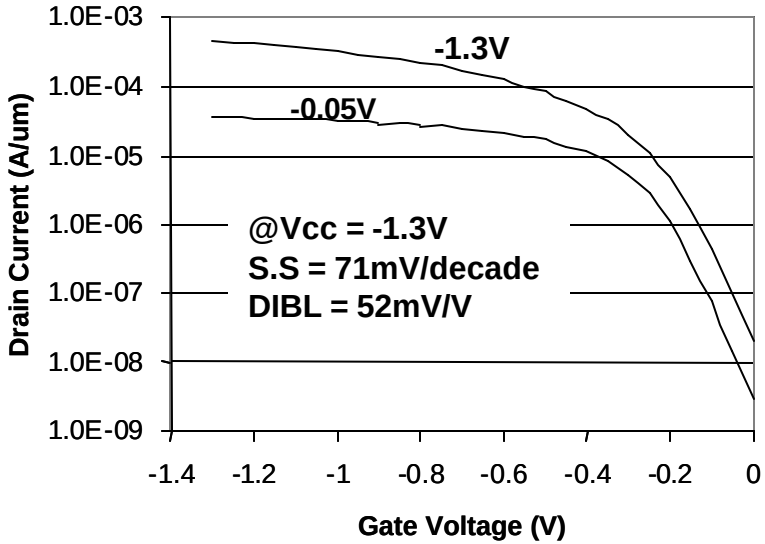
- **Taller T_{Si} than single-gate; shorter T_{Si} than double-gate**
- **Wider W_{Si} than double-gate**

Tri-gate DST Relaxes Si Body Dimensions



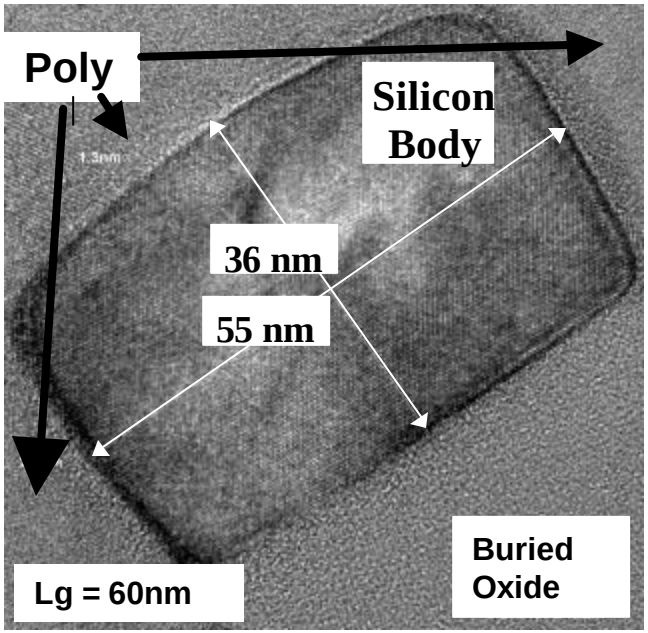


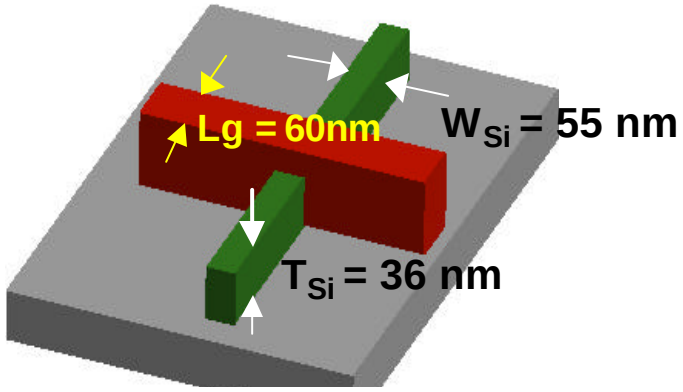




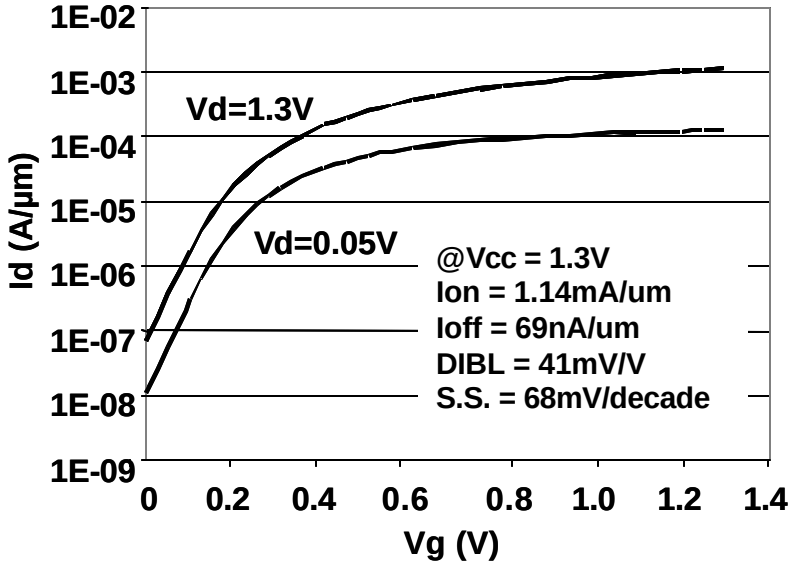
- **Tri-gate relaxes Si body dimensions: 2.3X thicker T_{Si} than single-gate DST, and ~2X wider W_{Si} than double-gate FINFET**

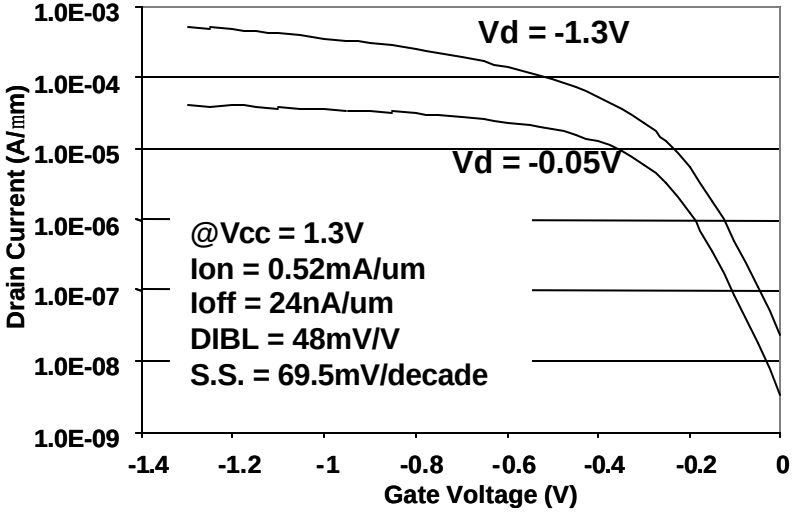
High-Performance 60nm Tri-gate DST CMOS





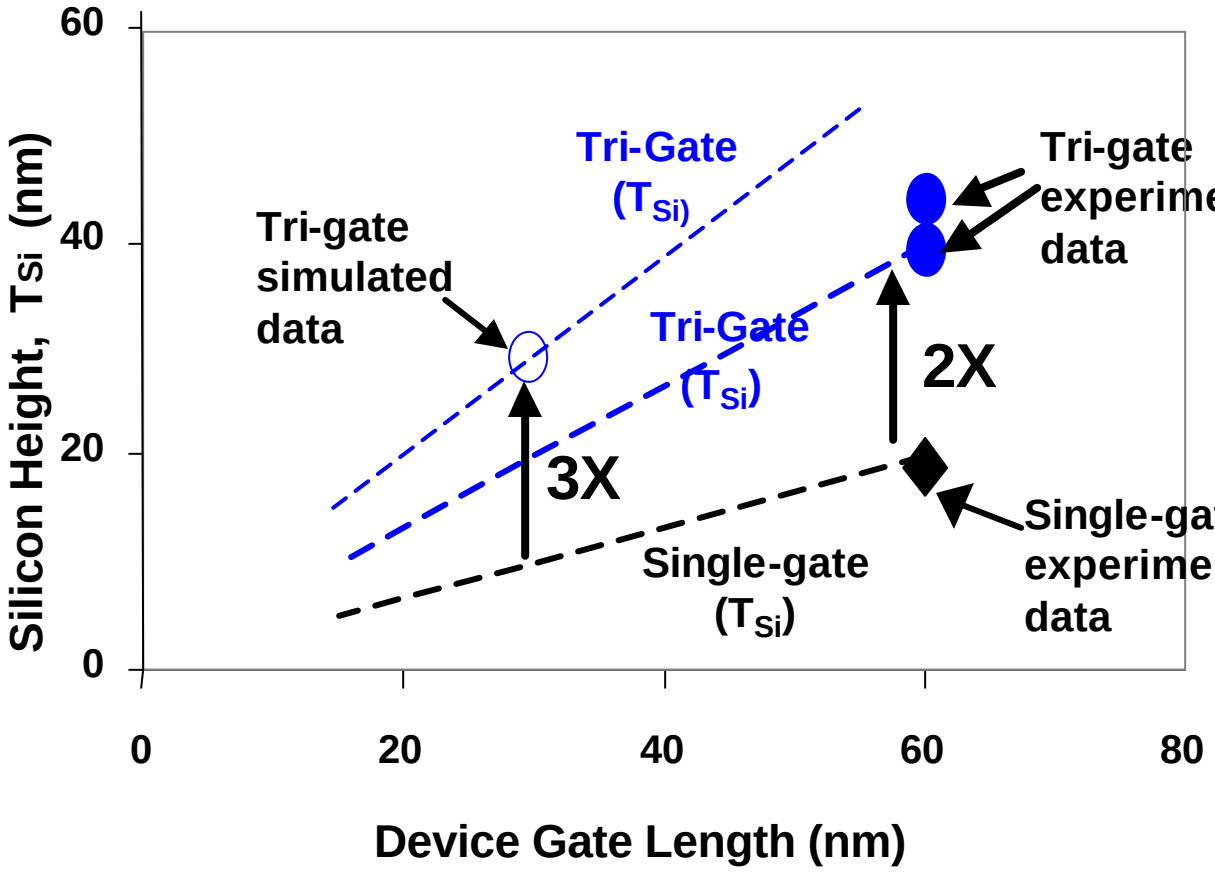
Current per unit width = $I_d/(2*T_{Si}+W_{Si})$

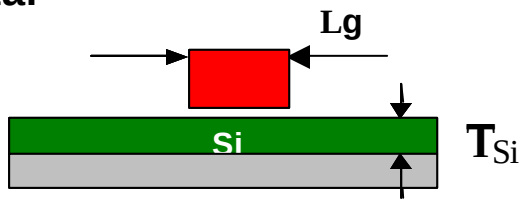


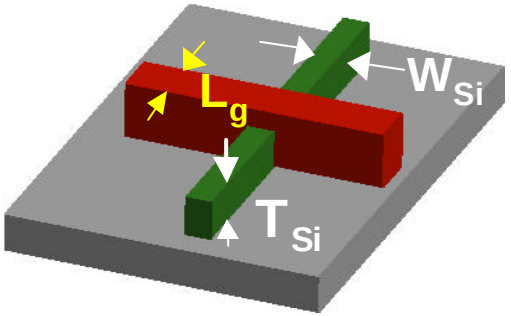


Highest NMOS and PMOS drive current performance ever reported for non-planar CMOS devices

Tri-gate Relaxes T_{Si} Requirement of Single-gate

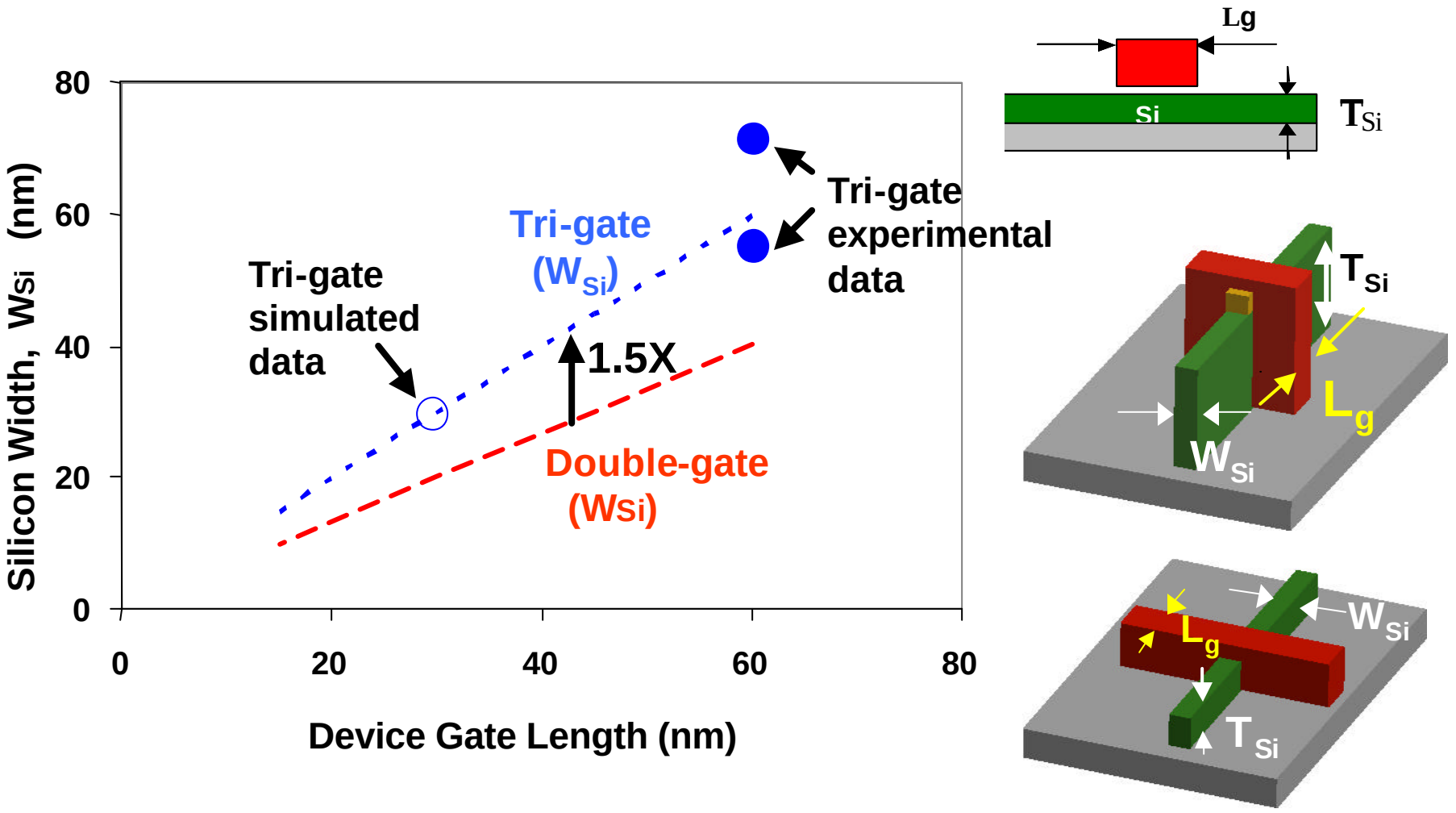






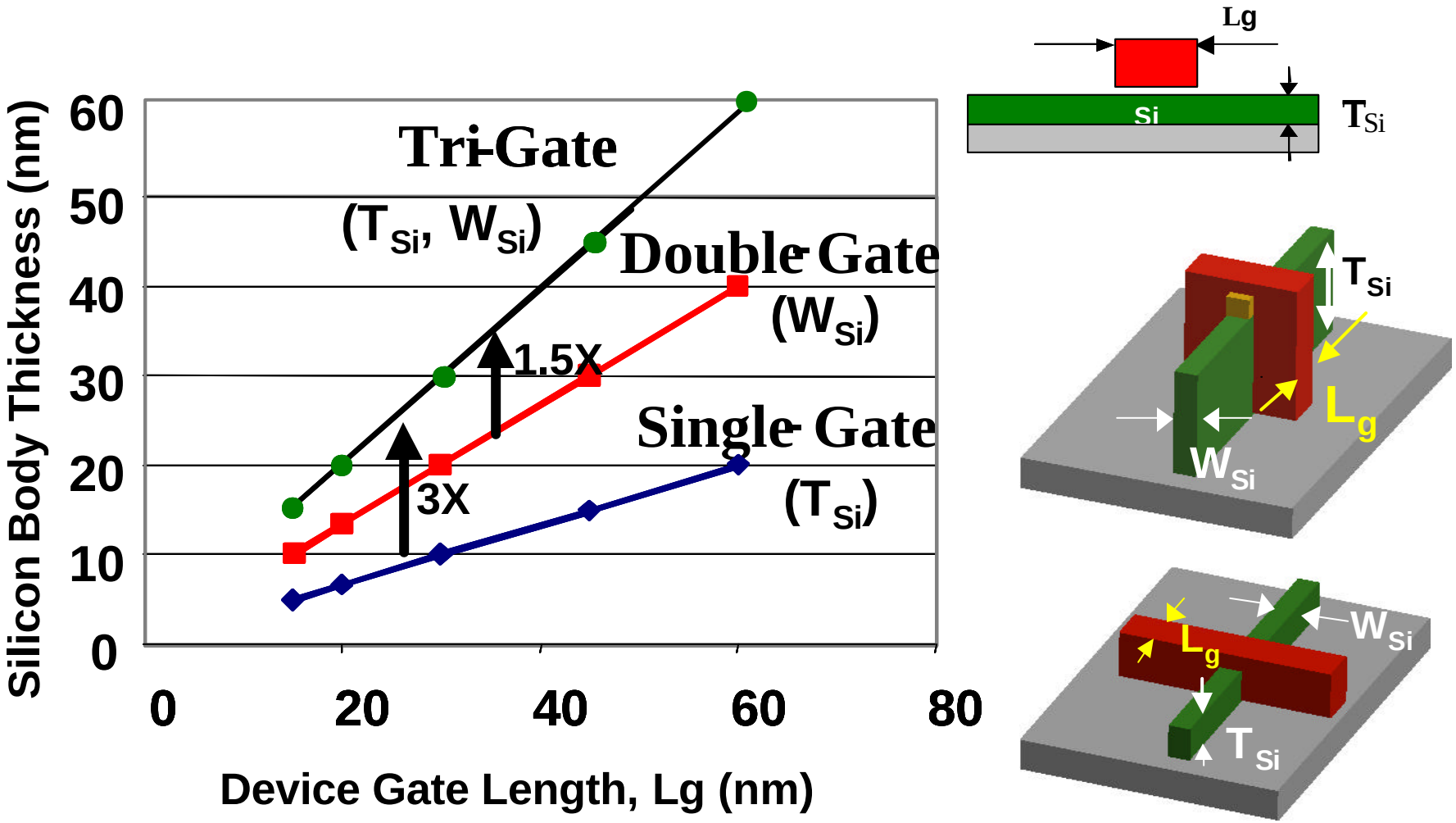
- **Tri-gate relaxes the T_{Si} requirement by 2-3X compared to single-gate**

Tri-gate Relaxes W_{Si} Requirement of Double-gate



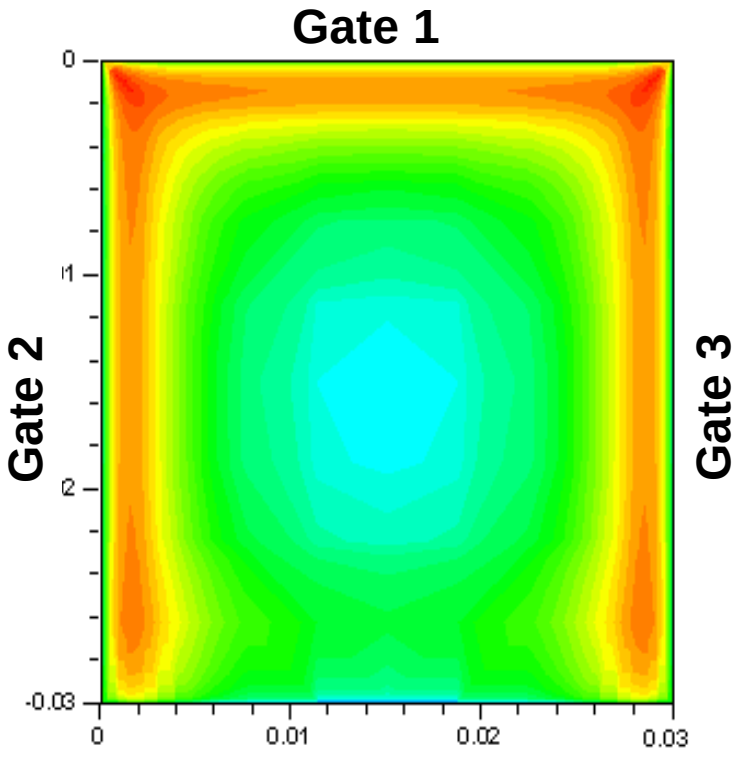
- Tri-gate relaxes the W_{Si} requirement by >1.5X compared to double-gate

Tri-gate has Least Stringent Thickness & Width Requirements

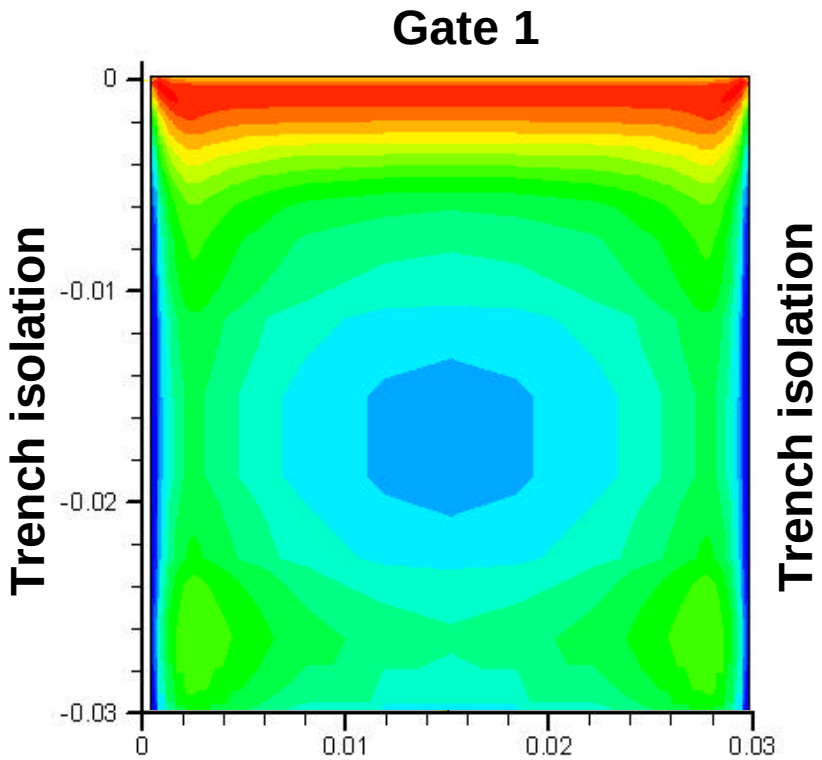


Tri-gate with $W_{Si} = T_{Si} = L_g$ = 30nm @ Vcc=1V

Computer Simulations (Channel Current density)



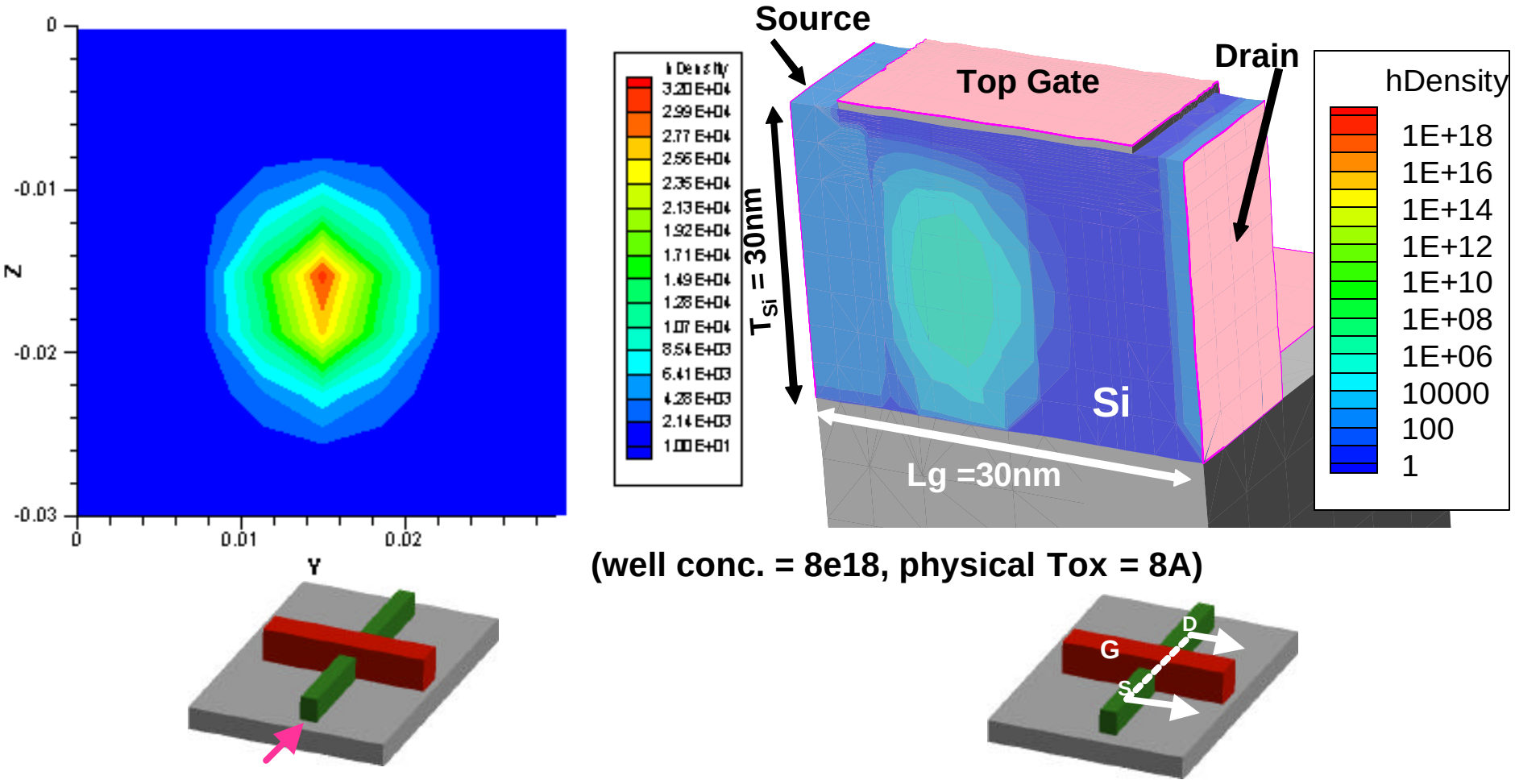
Tri-gate



Single-gate SOI

- All 3 gate electrodes control the channel current flow

Simulations of W_{Si} = T_{Si} = Lg = 30nm @ Vcc=1V

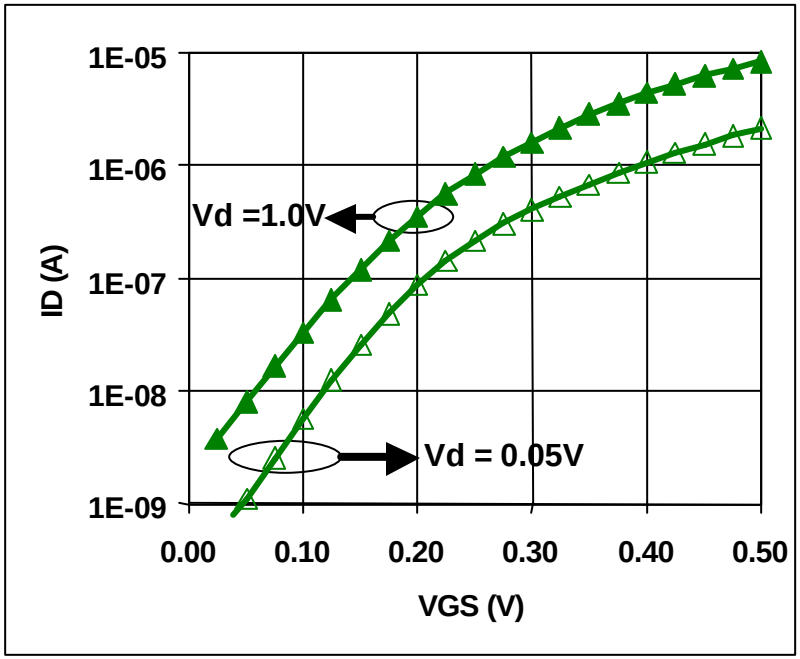


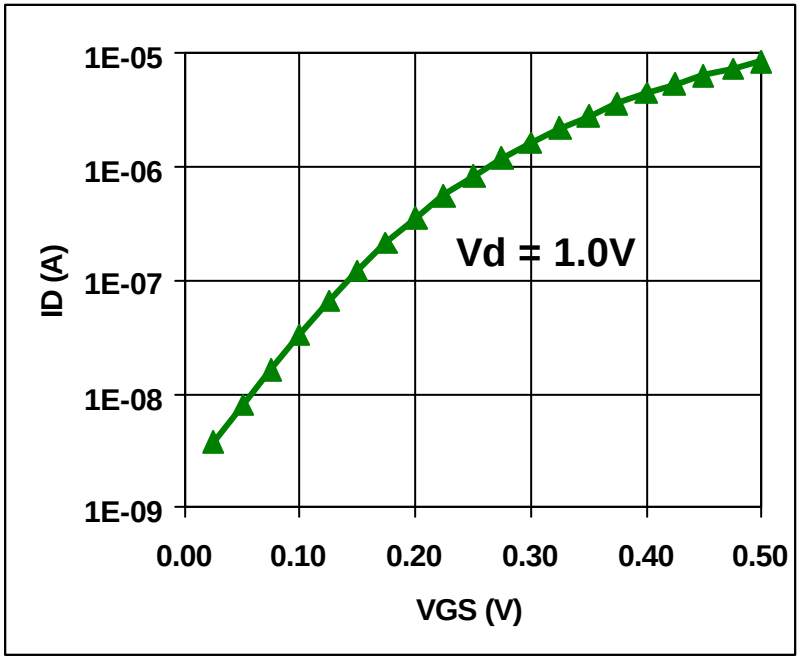
(well conc. = 8e18, physical Tox = 8A)

- **All 3 gates control the depletion regions in the tri-gate device**

Tri-gate with $W_{Si} = T_{Si} = L_g = 30nm$ (Computer Simulations)

(well conc. = 8e18, physical Tox = 8A)

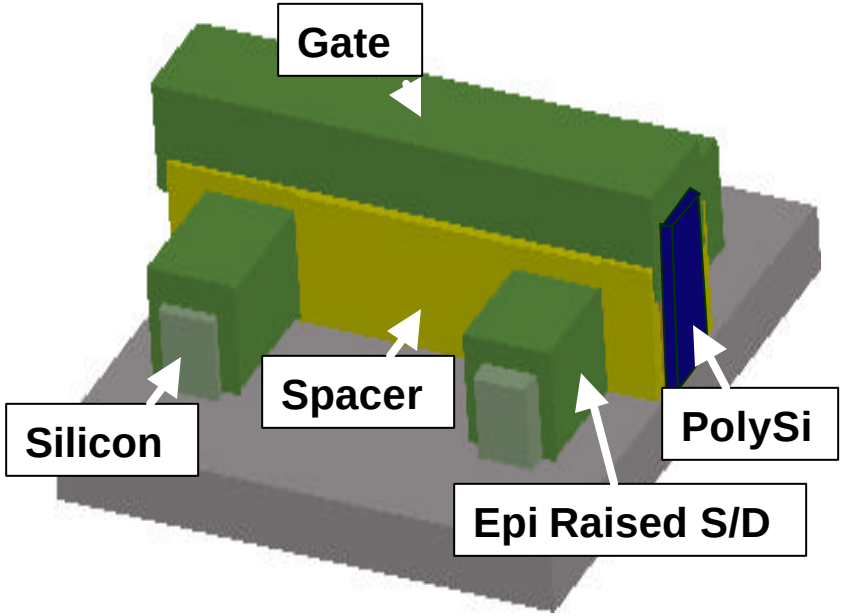


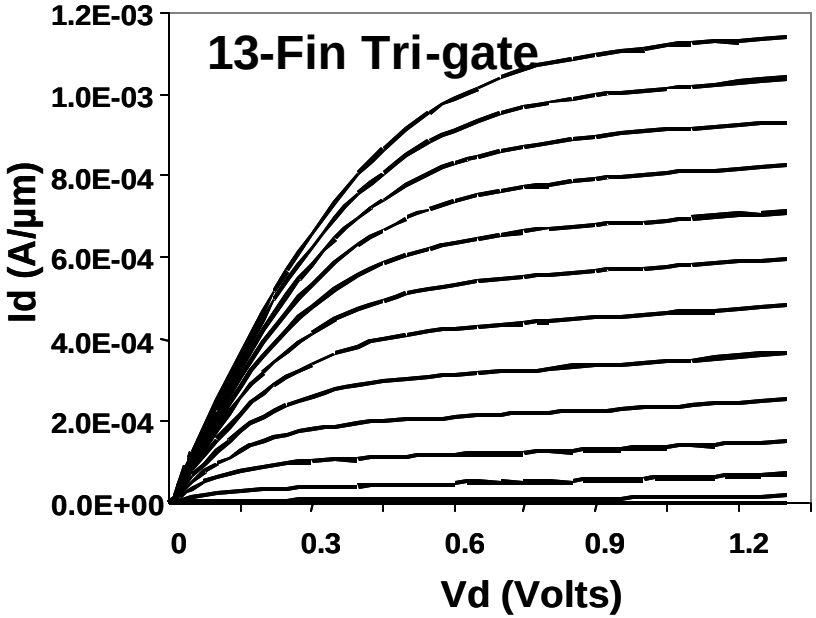


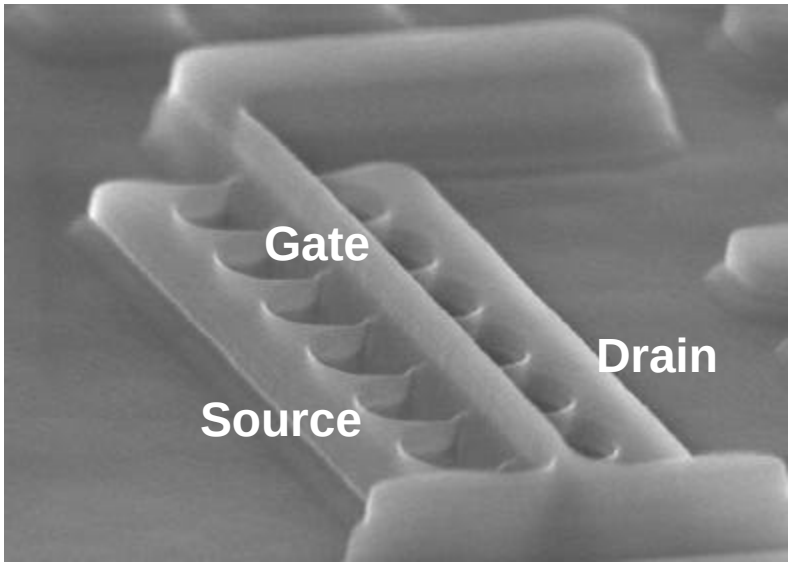
DIBL = 71mV/V

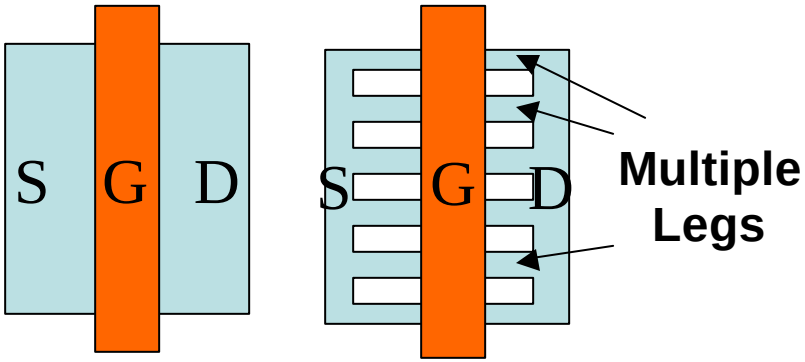
S.S. = 63mV/decade

Multiple-Leg Tri-gate Transistor to Increase Total Current



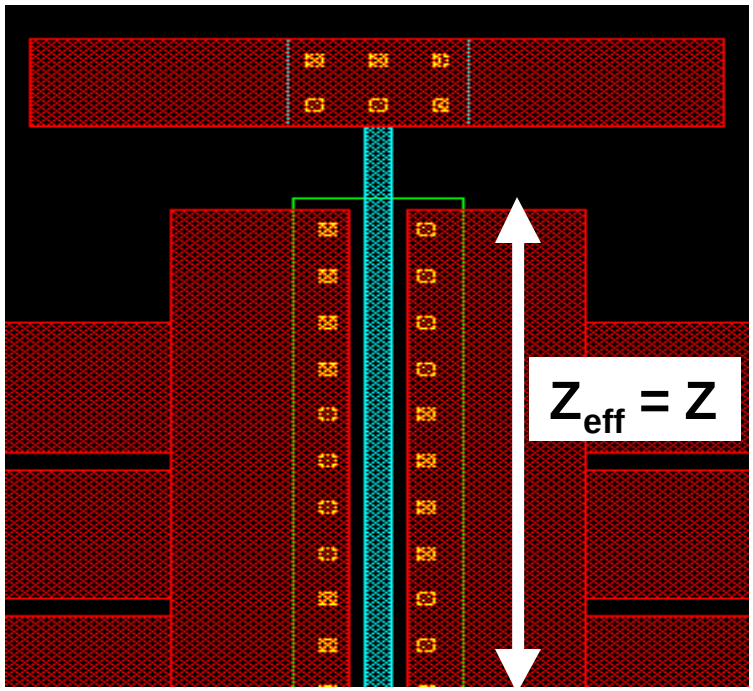




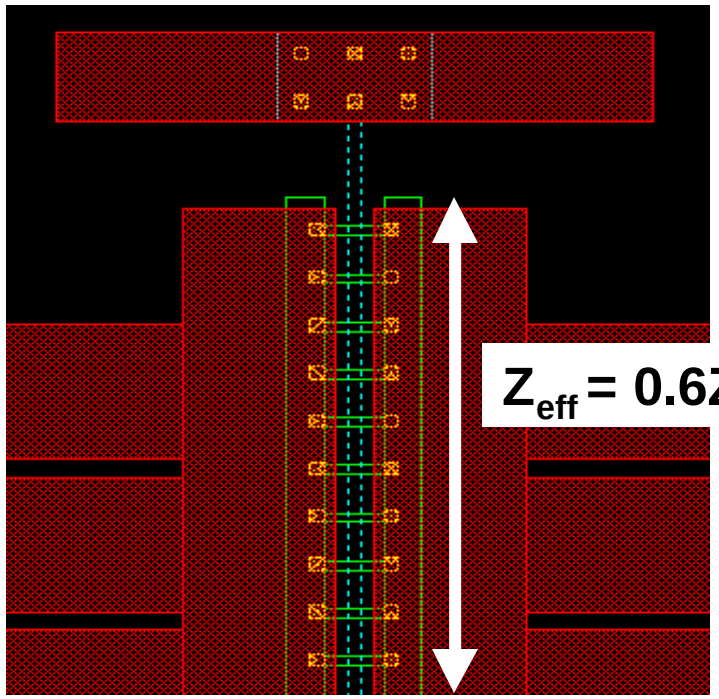


Total Drive Current =
I_d per Tri-gate Transistor x no. of Legs

Layout Considerations



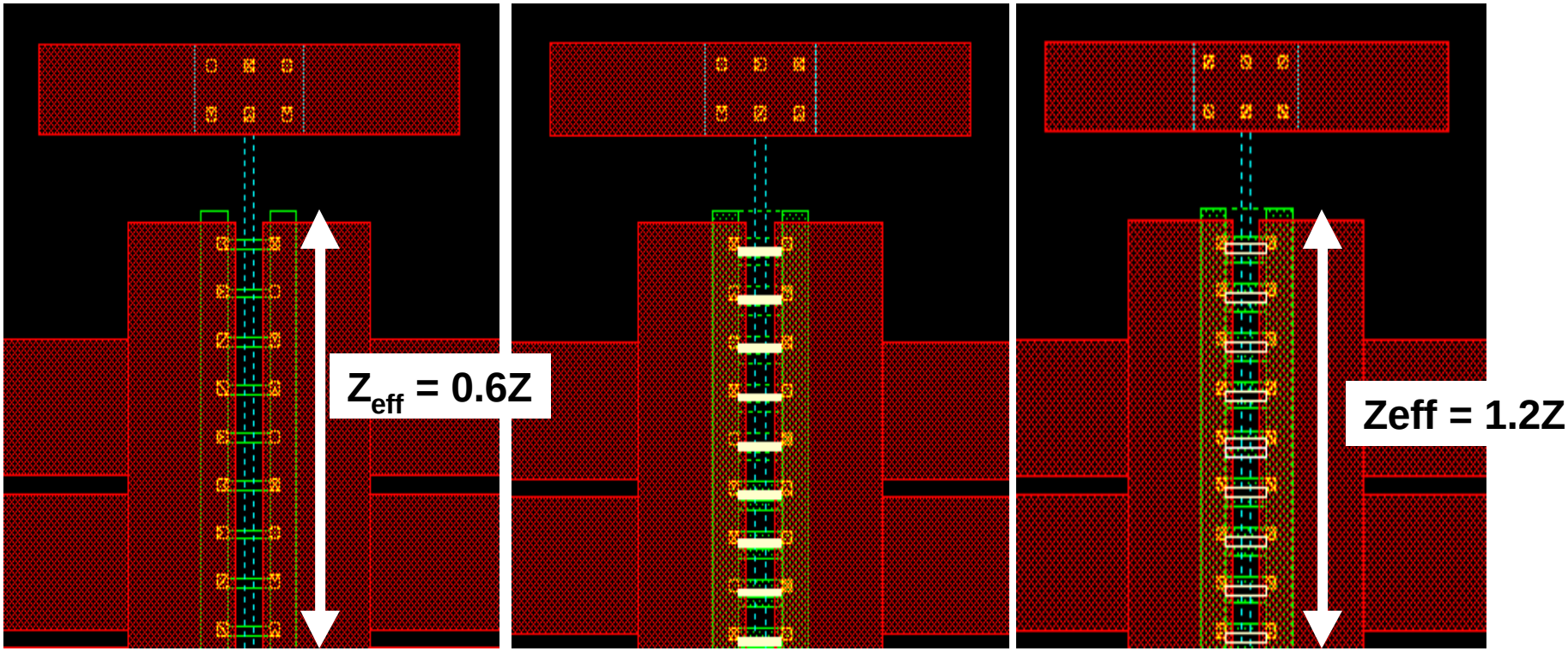
Standard Transistor



Tri-Gate Transistor

- For a given pitch, total current per unit layout-width of the tri-gate transistor is only 0.60X of that of the standard transistor
- Need to use spacer-gate technique to double the # of fins for a given pitch to increase total current

Spacer-Defined Fins



Litho-defined Fins

Oxide blocks to define spacer-masks for forming Si fins

For the same pitch, # of spacer-defined fins doubles that of litho-defined fins

- Use of spacer gate technique enables the tri-gate transistor to have 20% more total current per unit layout-width than the standard transistor

Conclusions

- **Compared to single-gate and double-gate, tri-gate fully-depleted CMOS transistors relax the silicon height and width requirements**
- **Tri-gate CMOS with Lg = 60nm fabricated and shown highest ever reported NMOS and PMOS drive performance for non-planar devices**
- **Tri-gate fully-depleted CMOS exhibits much better short-channel effect (sharper subthreshold slope and smaller DIBL) than standard bulk CMOS**
- **Tri-gate CMOS with spacer-defined fins has potential to provide 20% higher total current per unit layout area than standard bulk CMOS**